20-Mode Universal Quantum Photonic Processor

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Integrated photonics is an essential technology for optical quantum computing. Universal, phase-stable, reconfigurable multimode interferometers (quantum photonic processors) enable manipulation of photonic quantum states and are one of the main components of photonic quantum computers in various architectures. In this paper, we report the realization of the largest quantum photonic processor to date. The processor enables arbitrary unitary transformations on its 20 input modes with an amplitude fidelity of $F_{\mathbf{Haar}} = 97.4\%$ and $F_{\mathbf{Perm}} = 99.5\%$ for Haar-random and permutation matrices, respectively, an optical loss of $2.9\,\mathrm{dB}$ averaged over all modes, and high-visibility quantum interference with $V_{\mathbf{HOM}} = 98\%$. The processor is realized in Si_3N_4 waveguides and is actively cooled by a Peltier element.

1 Introduction

Photonics is one of the most attractive approaches to quantum computing, having gained momentum thanks to recent experimental results demonstrating a quantum advantage in photonics [1, 2]. The strengths of photonic quantum computing platform are as follows: first, quantum states of light are characterized by inherently low decoherence due to their weak interaction with the surrounding environment; second, photonic quantum states maintain their coherence at room temperature; third, photonic quantum computing can exploit the high maturity of existing classical integrated photonics technologies. These factors together mean that integrated photonics represents a scalable approach to large-scale quantum computing. Finally, photons are the natural solution for constructing quantum networks for either distributed quantum computing or for quantum communication [3, 4, 5, 6].

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Quantum computational models based on photonics range from non-universal approaches, such as Boson Sampling [7], which forms the basis of the recent quantum advantage experiments [1, 2], to universal ones based on a variety of different encodings [8, 9, 10, 11, 12, 13]. Applications of non-universal photonic quantum computing have been proposed, such as quantum chemistry [14, 15] and graph properties [16].

Linear optics is at the core of photonic quantum computing, as it is the natural means to generate entanglement between photons. Despite the fact that photons are non-interacting particles, entanglement can be formed via quantum interference in a linear optical system, with the archetypal example being the Hong-Ou-Mandel effect [17]. One can place several requirements on a linear optical system for quantum interference. First, the system must be programmable and universal, in the sense that arbitrary optical transformations can be set by the user, with high fidelity. Second, low losses are also a prerequisite for photonic quantum computing as otherwise the information carried by quantum light is lost. Third, the linear optical system must be large in scale, to increase the complexity of the calculation that can be performed.

Integrated photonics has become essential for photonic quantum computing [18] as it represents a scalable, mature and commercially available tool to realize large-scale, inherently phase-stable and fully-reconfigurable linear optical interferometers, called a Quantum Photonic Processor (QPP) in this context. A quantum photonic processor [14, 19, 20, 21, 22] is one of the essential components of photonic quantum computing and is the main player in applications such as quantum neural networks [23], quantum metrology [24], PUFs [25], witnesses of bosonic interference [26, 27] and for benchmarking multi-photon light sources [28, 29]. Of the available integrated platforms, stoichiometric silicon nitride Si_3N_4 is the most promising platform for photonic quantum computing. It provides an optimal combination of low loss and high optical mode confinement [30], enabling the scal-

ing up of low-loss fully-reconfigurable linear optical interferometers for quantum computing and information processing.

In this paper, we present the largest universal quantum photonic processor to date, with 20 input/output modes. Throughout this paper, 'modes' refers to the input/output waveguides of the processor, supporting only the fundamental optical mode. We note that each waveguide supports optical modes at multiple frequencies.

Our processor is based on stoichiometric silicon nitride Si_3N_4 waveguides using TripleX technology [31] and is backed with a water-cooled Peltier element to maintain a constant temperature. The waveguides are realized with an asymmetric double-stripe cross-section and have a minimum bending radius of 100 μm. The device has losses of 2.9 dB averaged over all modes and enables arbitrary linear optical transformations, making it compatible with all linear optical models of quantum computation. We test the reconfigurability of the processor over more than 1000 unitary transformations, and show a high degree of control of the linear optical interferometer, as well as its universality. We further validate the processor with 190 quantum interference experiments confirming that the processor preserves the properties of quantum light at each of its components.

2 The Quantum Photonic Processor

Our 20-mode quantum photonic processor consists of three parts: the Si_3N_4 photonic chip, the peripheral system which includes the control electronics, and dedicated control software [22]. The Si_3N_4 photonic chip (Fig.1a) contains a total of 380 thermo-optic tunable elements, arranged in a universal square interferometer (Fig. 1b) where the unit cell comprises a tunable beam splitter (TBS) followed by a phase shifter (PS) [32]. Propagation losses as low as 0.07 dB/cm at 1562 nm are measured across the entire photonic chip, obtained by a higher-temperature annealing process compared to our previous chip [22]. The peripheral system comprises the control electronics and an active cooling module. The thermo-optic tunable elements can be switched at kHz rate [30], setting the limit for the switching speed between different configurations of the processor. To precisely control the temperature of the photonic chip, it is actively cooled. The cooling module consists of a Peltier element attached to a water cooling module providing a maximum heat reduction rate of 200 W.

The dedicated control software performs both the decomposition of any unitary matrix transformation into the phase settings of each unit cell and their assignment to the corresponding tunable elements. The control software takes also into account the imperfections of the processor, such as crosstalk of individual tunable elements and compensates for those.

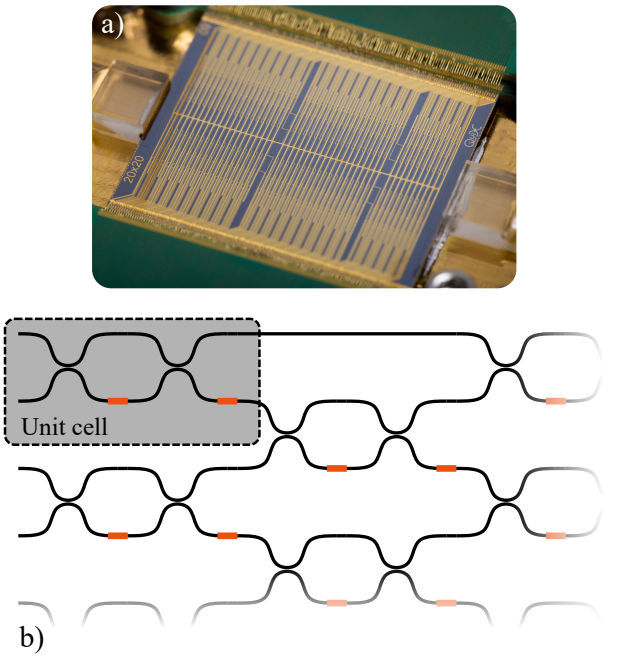

Figure 1: **a)** Photograph of the 20-mode processor chip (22 mm × 30 mm). The chip is optically packaged to an input/output fiber array and it is wire-bonded to the control PCB enabling the addressing of each individual tunable element. **b)** Functional design of the processor displaying the outline of the thermo-optic tunable elements (in red) and ideal layout of the waveguide paths (in black). The mesh is built by repeating the unit cell, comprising a tunable beam splitter (TBS) and external phase shifter (PS), $\frac{1}{2}N(N-1)$ times where $N = 20$ for a total of 190 unit cells.

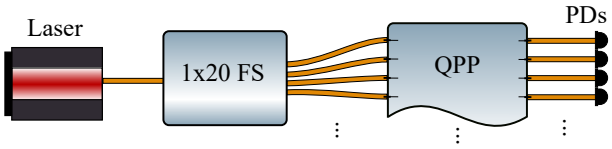

Figure 2: Sketch of the experimental setup for classical characterization of the processor. Laser: Santec TSL-570, FS: fiber switch Fibermart 1×32 PM, PDs: Thorlabs FGA01FC

3 Experimental Results

In order to demonstrate the suitability of our processor for photonic quantum computing, we demonstrate full reconfigurability and control, as well as preservation of quantum interference across the whole 20-mode linear optical interferometer.

3.1 Classical Results

The full control of the processor is demonstrated by characterizing the phase-voltage relationship of each thermo-optic actuator. This step is performed by injecting coherent light into the 20-mode processor via a 1×20 PM fiber switch (Fig. 2).

Each tunable element is driven to discrete voltage values and its output power is recorded at a photodi-

ode array (PDs) and processed by the control software to obtain the true phase response of each tunable element. The characterization of the 380 tunable elements shows that they all have a phase tuning range exceeding 2π, allowing for full control of the unitary transformation implemented within the interferometer. The insertion loss of the photonic processor is measured to be (2.9 ± 0.2) dB: this is the overall loss experienced by light going in and out of the processor, from input to output fiber, through all the tunable MZIs and phase shifters. The measured insertion loss corresponds to coupling and propagation loss of, respectively, 0.9 dB/facet and 0.07 dB/cm.

Finally, we verify the reconfigurability and control of the processor by generating and implementing 190 permutation and 1000 Haar-random matrices on the device. Generating Haar-random unitary matrices is done via the method proposed in [33]. For each input mode of the permutation and Haar-random matrices, the output intensity distribution is measured. From this distribution, a fidelity measure $F = 1/N \ \mathrm{Tr}(|U^+| \cdot |U_{\mathrm{exp}}|)$ of the unitary optical transformations on the input light is determined, where $|U|$ refers to the component-wise absolute value and where $N = 20$ is the number of modes. This fidelity measure is typically referred to as the amplitude fidelity. We obtain such fidelities as high as $F = (99.5 \pm 0.2)\,\%$ and $F = (97.4 \pm 0.5)\,\%$, for the permutations and the Haar-random transformations, respectively (see also Fig. 3a and b).

As an example, Fig. 3c shows a comparison between one of the target Haar-random matrices (left), and the measured results from the implementation of that matrix on the QPP (right). The strong resemblance between the two plots can be clearly seen, as confirmed by the matrix plot in Fig. 3d showing that the error on the implemented amplitude matrix elements falls within 0.2.

We note that the processor's performance remains stable for at least 6 months, i.e., there is no need of re-calibrating the device for at least half a year. This is due to the stability of the on-chip structure and control electronics.

3.2 Quantum Results

Measuring the visibility of HOM interference [17] at every location on the processor provides quantum validation of the device. In order to do so, we use a photon-pair source based on degenerate Type-II spontaneous parametric down-conversion (SPDC) in periodically poled potassium titanyl phosphate (PPKTP). Pumped at 775 nm with picosecond pulses, pairs of photons are generated with low probability on each pulse. The generated photons are highly indistinguishable and frequency-unentangled, with a mutual Schmidt number of about 1.1. For this experiment, the photons are filtered to $\Delta\lambda \approx 12$ nm using bandpass filters, to ensure maximum purity of the two-photon state. The photons are collected by optical fibers. Partial temporal distinguishability between the photons can be continuously tuned by varying the relative path length of the photons using a motorized linear displacement stage.

The photons are then injected into pairs of input modes, as in Fig. 4, and are routed to interfere at each on-chip TBS, set to a 50:50 splitting ratio. The output modes are connected to superconducting nanowire single-photon detectors (SNSPDs), whose coincidence rate is measured using a standard time-tagger.

In order to route the two photons to every on-chip TBS, and to the connected outputs, the entire interferometer is used. TBSs are set to full reflection or transmission to create optical paths, which contain no intersections other than the TBS of interest. The normalized HOM dips at all 190 TBS are reported in Fig.5a: the clear overlap of all plots shows that the processor preserves the indistinguishability of the input single photons, as can be also seen in the low spread of the visibility histogram in Fig. 5b. The spatial distribution of the HOM visibilities over the rows and columns of the processor, as shown in Fig.5c, is quite random, confirming that there are no systematic errors within the processor. Furthermore, the visibility of the HOM interference appears to be limited by the quality of the source used for the characterization.

To preserve the quantum interference, it is important that the overlap between photons remains as high as possible. Any path length difference, either geometrical or optical, will lower this overlap. In multi-photon experiments, single photons can interfere not only on a specific TBS but also across the entire processor via different paths that might be quite different from each other. It is thus important to quantify the effect of on-chip path length differences.

To assess this, we measure the path length differences that our processor induces over a long on-chip path, given by the shift of the HOM interference dip obtained by injecting two single photons in the top two inputs and measuring their coincidences at the bottom two outputs, i.e., over the main diagonal of the processor. The induced path length difference is varied by sweeping the voltage of every phase shifter on one of the arms of the main diagonal. This induced path length difference could be observed as a shifting of the HOM dip positions, see Fig.5d and Fig.5e. A shift of more than 60 µm is measured, or a maximal phase shift of at least 3π per heater. Depending on the coherence length of the photons, this temporal delay can induce a strong effect on the indistinguishability of the photons.

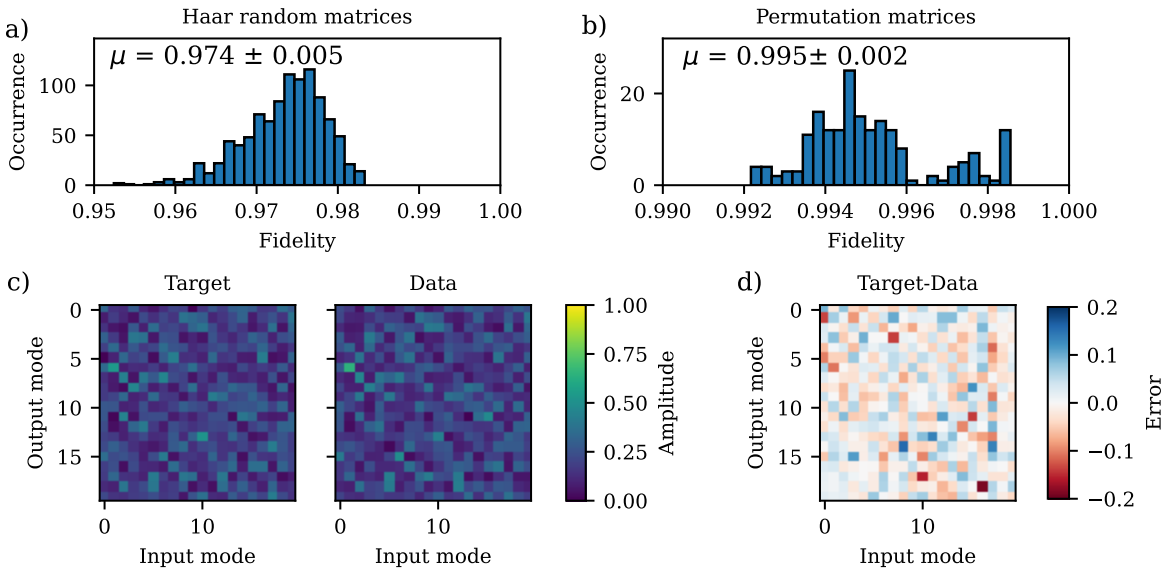

Figure 3: Summary of the classical characterization. **a)** and **b)** Distribution of the measured amplitude fidelities for, respectively, 1000 Haar-random matrices of average fidelity $(97.4\pm0.5)\,\%$ and 190 Permutation matrices with average fidelity $(99.5\pm0.2)\,\%$. **c)** Comparison between the amplitude distribution of an ideal Haar-random unitary matrix (target) with its experimental implementation (data). **d)** Difference between the target and the measured (data) Haar random matrix.

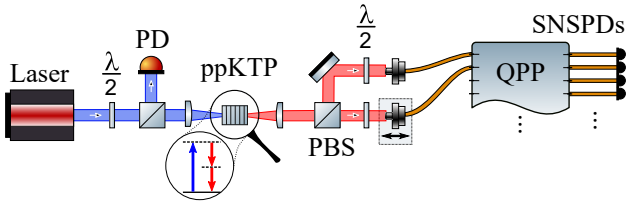

Figure 4: Sketch of the experimental setup for quantum characterization of the processor. A Ti:Sapphire laser is used to pump a ppKTP crystal, producing a pair of degenerate photons. The photons are injected into the processor where HOM interefence is tested. Each output mode is connected to an SNSPD.

	N	IL (dB)	CL (dB/facet)	PL (dB/cm)
12-mode	132	5	2.1	0.1
20-mode	380	2.9	0.9	0.07

Table 1: Comparison between the 12-mode [22] and 20-mode processor. N = number of thermo-optic phase shifters, IL = Insertion Loss, CL = Coupling Loss, PL = Propagation Loss

4 Discussion and Conclusions

The current quantum photonic processor distinguishes itself from its predecessor [22] in several ways (Table 1). On the hardware level, we increased the number of optical input and output modes from 12 to 20. Despite its greater size and the increased optical path lengths per mode, the insertion loss is significantly reduced to an average of $(2.9 \pm 0.2)\,\mathrm{dB}$. This reduction stems mostly from improved fiber-to-chip coupling with an average coupling loss of $0.9\,\mathrm{dB/facet}$.

A quantum photonic processor is at the core of a photonic quantum computer. Crucial properties of a QPP include its full programmability and universality, which we demonstrate in this work. Other critical properties for optimal quantum processing are low losses and large scale, i.e., large number of unit cells. These two features are not always compatible with each other as usually high-index-contrast high-confinement material platforms that enable the densest optical circuits (largest number of unit cells on a wafer), such as SOI or InP, suffer from greater losses (both propagation and coupling) than other platforms, such as silicon nitride (SiN) or silica. On one hand, this is due to the strong interaction of the optical mode with the sidewall surface roughness and, on the other hand, to the large optical mode mismatch at the facets of the chip. In the next paragraphs we discuss and show the SiN technology as the best platform for realizing universal quantum photonic processors. SiN is in fact capable of satisfying the requirement of large-number of modes while, at the same time, providing ultra-low losses.

If we locate our work in the context of universal photonic processors, i.e., fully-reconfigurable and all-to-all connectivity, it can be clearly seen that our systems provide the highest number of input/output modes for the lowest insertion losses (Fig.6). Insertion losses, in this case, include both coupling and on-chip losses. This confirms the prominence of silicon nitride technology as mature platform for realizing universal quantum photonic processors. The data points in Fig.6 come from [19, 34] for silica, [21, 22, 35, 36] for SiN and [20, 37, 38, 39] for silicon-on-Insulator. Other impressive works of large-scale photonic integrated circuits can be found in the literature, however they are either non-universal or have unknown

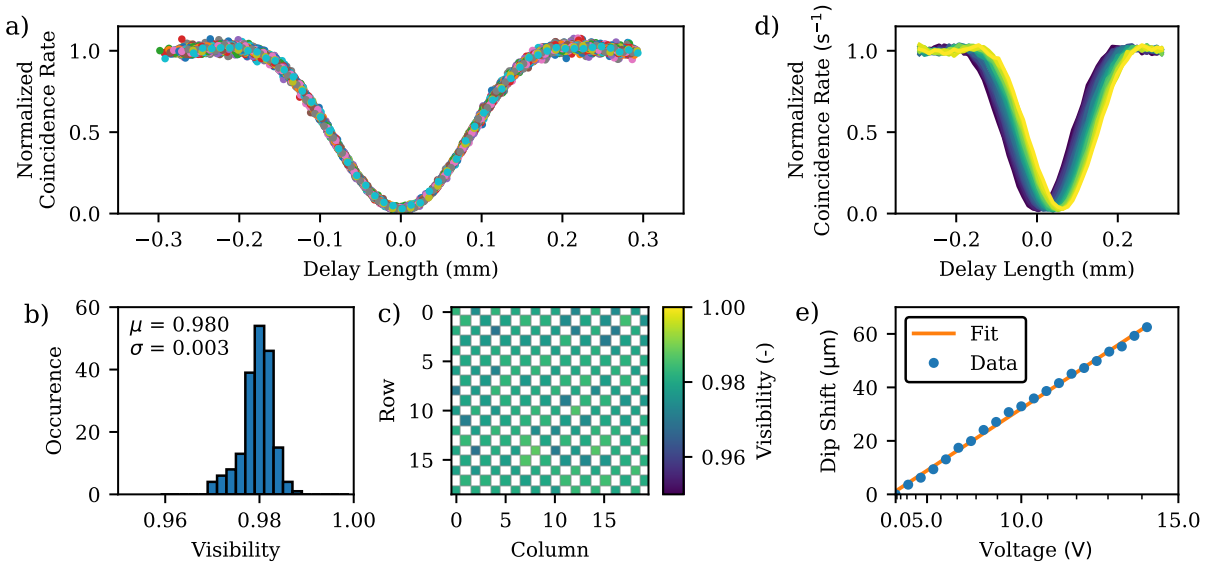

Figure 5: Results of the HOM interference measurements for all TBS on the processor. **a)** The normalized coincidence rates of all TBS in the processor; 190 separate interferograms are shown. A Gaussian fit was used to determine the visibility of the HOM interference. **b)** Histogram of the HOM visibility of all TBS in the processor. **c)** HOM visibilities of all TBS for each processor row and column. The checkerboard pattern reflects the alternating pairwise coupling of neighbouring channels as laid out in Fig. 1b. **d)** Normalized coincidence rates for various delays induced by increasing voltages across the main diagonal. **e)** Total path length tunability of the longest diagonal path across the matrix.

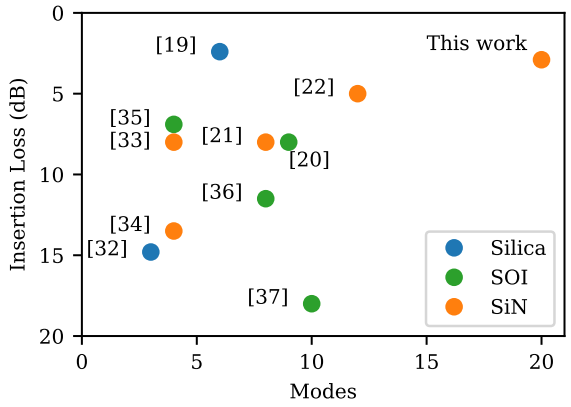

Figure 6: Overview of universal photonic processors performances as reported in the literature. We plot the insertion loss of each processor versus the number of optical modes of the largest universal transformation as in [32] that can be implemented within each processor. Insertion loss includes the on-chip propagation loss and twice the fiber-to-chip coupling loss.

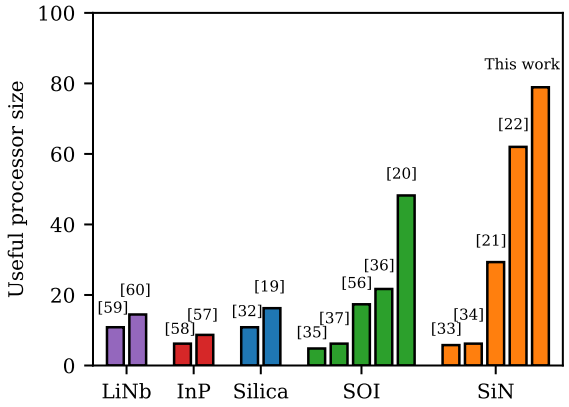

Figure 7: Overview of the useful processor size for various material platforms. We consider the loss per unit cell of each cited paper and plot the number of unit cells that can be sequentially concatenated before reducing the transmission to e^{-1}.

performance in terms of losses [40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 20, 53, 54, 55, 56, 57].

Scalability is another crucial property to consider when dealing with large-scale universal photonic processors. On-chip propagation losses are to be considered the main limiting factor. In particular, if propagation losses are too high, no useful universal processors can be realized. In order to compare the scalability of various material platforms, we report in Fig.7 the achievable processor size before reaching an arbitrary loss value, i.e., the useful processor size. We take

the loss per unit cell of various processors as found in the literature and calculate the processor size at which the transmission is reduced to an arbitrary threshold, in this case e^{-1}. The reader should note that computing or information processing protocols have different transmission thresholds. The reader should also note that the useful processor size in Fig.7 is based on the current state of the art and should therefore not be considered the absolute upper limit: as the loss per unit cell decreases, the useful processor size increases. The data points in Fig.7 are the same as in Fig.6 with the addition of [58] for SOI. For completeness of the overview, we include data points for active materials such as indium phosphate [59, 60] and lithium niobate [61, 62]. Fig.7 clearly shows that given an arbitrary loss, SiN is the most scalable platform allowing for the largest useful processor size.

Silicon nitride is also a highly versatile platform enabling on-chip quantum light sources [63, 64, 65], fast switching [66], lowest propagation losses [67] and superconducting single-photon detectors [68, 69]. Together with the highest capability of large-scale linear optical interferometer, as shown in this work, silicon nitride presents itself as a viable path to fully integrated quantum computers.

In conclusion, we have demonstrated a record universal quantum photonic processor with 20 input/output modes, which is the largest processor to date. Thanks to its low loss and high fidelity operations, it is the pinnacle of all universal quantum photonic processors demonstrated thus far.

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A

We report the measurements of the insertion loss for each mode of the processor. Light is injected at each $input_i$ and detected at its corresponding $output_i$. To achieve this, each unit cell of the processor is set to have output light in the same waveguide as the input.

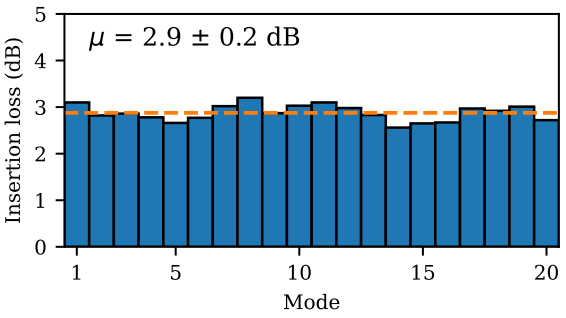

Figure 8: Bar plot of the insertion loss per mode number.

B

A Gaussian fit of a single HOM dip is shown where a baseline was establish by taking the average of all points that were more than two standard deviations away from the center of the dip.

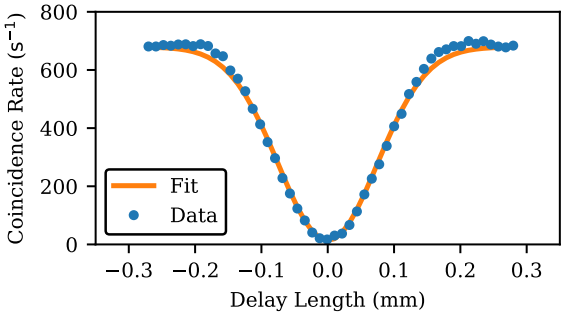

Figure 9: Example of a Gaussian fit for one of the measured HOM dips.

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